Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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S5	106	703/17.ccor.	US-PGPUB; USPAT	OR	ON	2006/02/02 17:36
S6	5	(("5754826") or ("5923567") or ("6197605") or ("6768983") or ("6891626")). PN.	US-PGPUB; USPAT	OR	OFF	2006/02/02 17:43
S7	24	optical adj digital adj profil$	US-PGPUB; USPAT	OR	ON	2006/02/02 17:43
S8	4	S7 and @ad<="20020228"	US-PGPUB; USPAT	OR	ON	2006/02/02 17:43
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#3	(((integrated circuit<and>simulat*)<and>profile) <and> (pyr >= 1951 <and> pyr <= 2002)) <AND> (((attribute<and>metrology) <and>parameter) <and> (pyr >= 1951 <and> pyr <= 2002))	42
#4	((fabrication<and>critical dimension)<and>shape) <and> (pyr >= 1951 <and> pyr <= 2002)	182
#5	((((integrated circuit<and>simulat*)<and>profile) <and> (pyr >= 1951 <and> pyr <= 2002)) <AND> (((attribute<and>metrology) <and>parameter) <and> (pyr >= 1951 <and> pyr <= 2002))) <AND> (((fabrication<and>critical dimension)<and>shape) <and> (pyr >= 1951 <and> pyr <= 2002))	5

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device model parameters needed to **simulate** the behavior of the design in a detailed circuit
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www-mtl.mit.edu/Metrology/PAPERS/MPU-long.pdf

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sequential steps occur in a standard **integrated circuit** development and production flow. Design:
etc.It is now standard to use ECAD tools to **simulate** the behavior of any schematic design of an
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and program complex, high-speed, digital **integrated circuits** within their own work environments.
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also require less external memory for storage. The **profile** of the circuitry that is active on the array
drl4.eee.strath.ac.uk/papers/pl_ieee96.ps.Z

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realization of densely packed (mixed signal) **integrated circuits** is prevention of cross-talk via the
and currents in the substrate, either by **simulation** of a 3D resistance mesh of the complete
The resistivity varies, because of the doping **profile**, only in the direction perpendicular to the
donau.et.tudelft.nl/pub/space/doc/1995/iccad95.ps.Z

<u>Simulation-based Performance Analysis of Distributed Systems - Schwarz, al. (1997)</u> <u>(Correct)</u> <u>(3 citations)</u>
Ulrich Donath Fraunhofer-Institute for **Integrated Circuits** Design Automation Department Zeunerstrasse
time-consuming method is the construction of a **simulation** model which includes the different subsystems,
subsystems, the communication system, and the load **profile**. In particular, this approach seems to be very
www.eas.iis.fhg.de/sim/publications/papers/1997/006/paper.ps.gz

<u>REDO - Random Excitation and Deterministic.. - Grimaila, Lee.. (1999)</u> <u>(Correct)</u> <u>(2 citations)</u>
term defects to denote actual flaws in an **integrated circuit**, which introduce erroneous operation for
ATPG process [FERG91]In this case, the fault **simulation** engine is modified to allow the **simulation** of
process. Specifically, each site's fault detection **profile** is lost in modern fault simulators because they
dropzone.tamu.edu/techpubs/./1999/ece9902.ps.gz

<u>Finite Element Resolution Of The 3d Stationary.. - Pena, Bruguera, Zapata (1997)</u> <u>(Correct)</u> <u>(1 citation)</u>
devices is an essential tool for **integrated circuit** designers. These simulators lead to an
mapping problem. 1 Introduction The numerical **simulation** of semiconductor devices is an essential tool
electron and hole concentrations and the doping **profile**, and R is the recombination-generation rate.
ftp.ac.uma.es/pub/reports/1997/UMA-DAC-97-01.ps.gz

<u>Efficient Electrostatic and Electromagnetic Simulation Using.. - Kapur, Long</u> <u>(Correct)</u>
are often used to extract models of **integrated circuit** structures. This extraction involves
Efficient Electrostatic and Electromagnetic **Simulation** Using IES 3 Sharad Kapur David E. Long Bell
material variations (e.g.the doping **profile** of a MOSFET)the differential approach is
www.bell-labs.com/user/kapur/Papers/ieee98.ps.gz

<u>PARTICS: A PARallel Taskfarm for Integrated Circuit.. - Gaston, Alexander..</u> <u>(Correct)</u>
PARTICS :A PARallel Taskfarm for **Integrated Circuit** Simulators G.J. Gaston, W.J.C. Alexander,
for performing CPU intensive process and device **simulations**. The system gives an almost linear speed up is
more CPU intensive. The structure and doping **profile** calculated by process **simulation**, provide
ftp.epcc.ed.ac.uk/pub/tr/91/tr9108.ps.Z

<u>Modeling And Simulation Of High Speed Interconnects - Biswas (1998)</u> <u>(Correct)</u>
Chapter 1 Introduction 1.1 Motivation As **integrated circuit** processing technology marches relentlessly
Modeling And **Simulation** Of High Speed Interconnects By Baribrata
CMOS Inverter. 10 3.3 Vertical **Profile** of a two layer metal and a single layer poly
www.i3s.leeds.ac.uk/homes/MBS/vitae_theses/biswas_ms_1998.pdf

<u>Compact Model Specification of RF MOSFET with DC and AC Evaluations - Kolding (1999)</u> <u>(Correct)</u>
to fully exploit the flexibility inherent to **integrated circuit** design. Most CMOS manufacturing facilities
MOSFET layout can be used to give better **simulation** results by including layoutdependent
transistor into inversion [30]Hence, the doping **profile** of the well changes with depth making analysis
www.tele.auc.dk/risc/resource/r991005.pdf

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